D I G I T R O N S E M I C O N D U C T O R S

Junction Field Effect Transistor (JFET) HR flow

All parts are screened per MIL-PRF-19500, JANTX Level and the device detail specification. All testing is performed at room temperature, unless indicated otherwise. For testing at high and low temperatures, Group A testing is required.

	Test	Method	Conditions / Notes
1	**Temperature Cycling**	*MIL-STD-750 Method 1051*	Test condition C or maximum storage temperature, whichever less. 20 cycles, 10 minutes per extreme.
2	**Interim Electrical Testing**		DC parameters per device detail specification.
3	**High Temperature Reverse Bias Burn-in**	*MIL-STD-750 Method 1039*	Condition A. 160 hours at 150°C and 80% of rated $V_{GS.}$
4	**Final Electrical Testing**		DC parameters per device detail specification.
5	**Delta Calculation**		Delta parameters and limits per device detail specification.
6	**PDA Calculation**		10 percent defective allowed.
7	**Seal Test Fine Leak**	*MIL-STD-750 Method 1071*	Condition G or H
8	**Seal Test Gross Leak**	*MIL-STD-750 Method 1071*	Condition C

Notes:

1. Testing varies in accordance with the device detail specification.
2. Specific customer testing needs may be accommodated into any testing flow (selection tests, temperature requirements, special tests).

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